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Integrated time counter with 200 ps resolution

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Abstract

The integrated time counter on a single CMOS FPGA device is presented. A 200 ps resolution has been achieved in the measurement range 0 – 167 ms utilizing two-stage interpolation method. The maximum integral non-linearity of the embedded time-to-digital converters is 312 ps. After correction of the linearity error the standard measurement uncertainty below 140 ps was obtained. The Delay-Locked Loop (DLL) was used for indirect time stabilization of the delay elements.

1. Introduction

The integrated time counters designed in digital programmable devices utilize the tapped delay lines to improve the measurement resolution [1–5]. Using a single delay line, to achieve a 200 ps resolution within a 10 ns range (period of a 100 MHz reference clock), the line should contain at least 50 delay cells [1]. It is not possible to obtain identical propagation time in all cells of such a long delay line, and thus the linearity error of the interpolators can be significant. Long delay lines are also more sensitive to temperature and supply voltage variations. Possibly short delay lines should minimize these effects. This has become possible with the use of the two-stage interpolation method and CMOS ASIC technology [6]. The presented time counter with two-stage interpolation is integrated in a CMOS FPGA device and allows to obtain all advantages of the two-stage interpolation, while providing low cost and short design cycle.

2. Time counter

The integrated time counter has been designed on a single CMOS FPGA device (Fig. 1). The time interval measurement is based on the Nutt interpolation method [7] and utilizes a 24-bit coarse counter and two-stage fine interpolators in both START and STOP input channels.

The first interpolation stage consists of a 5-cell delay line, common for both interpolators. The average propagation time of the delay cell is about 2 ns. This provides 5 different phases of the 100 MHz reference clock for the associated D flip-flops (FFs). The first synchronizing signal is found by the 5-input OR gate, the output of which is fed as a strobe signal to the second

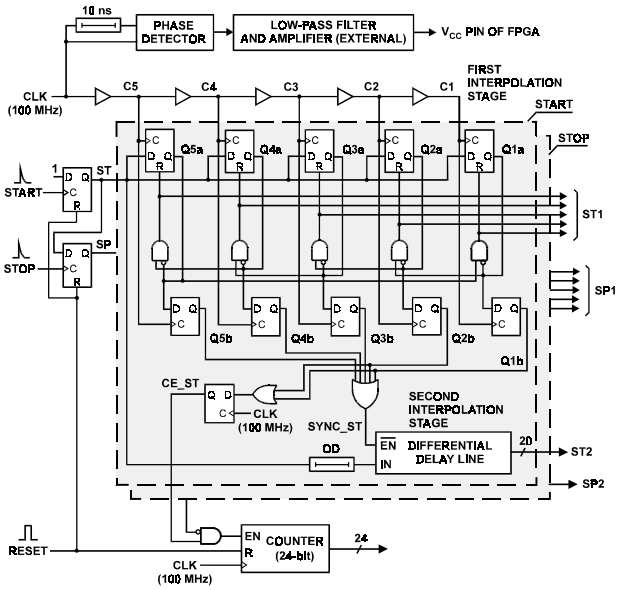

Fig. 1 Logic diagram of the time counter

interpolation stage. The phase difference between the synchronized signal and the input pulse (START or STOP) is measured by the second interpolation stage, where two tapped delay lines working in differential mode are used. The time resolution of that differential delay line is about 200 ps [1].

Since the input pulses (START and STOP) are asynchronous with respect to the reference clock (CLK), the risk of metastability is always present when FFs are used as phase detectors to produce the corresponding time intervals measured in the second interpolation stage. The used dual synchronizers significantly decrease the adverse influence of metastability effect [8], but also would add a CLK period T_0 to be measured by the second interpolation stage. The offset delay OD ($\sim T_0$) shortens the measurement range of the differential delay line to about 2 ns. Due to the technology spread additional 5 cells have been introduced at both ends of the line, which contains total 20 cells.

A right synchronization has to be used for control of the coarse counter operation. A commonly used method involves two counters clocked on rising and falling edges of the reference clock. When an input pulse occurs, at least one counter is in the stable state [4, 9]. Another method uses the double synchronization [10], where the input pulses are sampled at both edges of the reference

clock. The counter is sampled after one or two clock periods, consistently with the state present in the fine interpolation register. This method needs only four FFs and a two-input multiplexer for each interpolator.

In the presented time counter the control of the coarse counter is simply obtained by utilizing a D FF and a 2-input OR gate for each interpolator (one FPGA cell). The timing diagram for the START interpolator is shown in Fig. 2. The counting is always enabled with the delay $T_A + 2T_0 - \Delta t_{DL}$ after the input pulse (START). The time interval Δt_{DL} is the difference between the propagation time of the DLL delay line and the delay line used in the first interpolation stage. The same method is used for disabling the counter (in the STOP interpolator).

The time counter was realized on a FPGA device QL12X16B from the pASIC1 family, manufactured by *QuickLogic* in a 0.64 μm, 2-layer CMOS technology.

To stabilize the propagation time of delay elements against the temperature changes and aging, a delay-locked loop (DLL) controlling the FPGA supply voltage V_{CC} has been used [11]. A separate delay line in the first interpolation stage was introduced to lower the load at the buffer nodes of the DLL line and obtain the V_{CC} values within the permissible range for the used FPGA device. The power supply voltage of 5.48 V was achieved in the lock state of DLL at a normal room temperature.

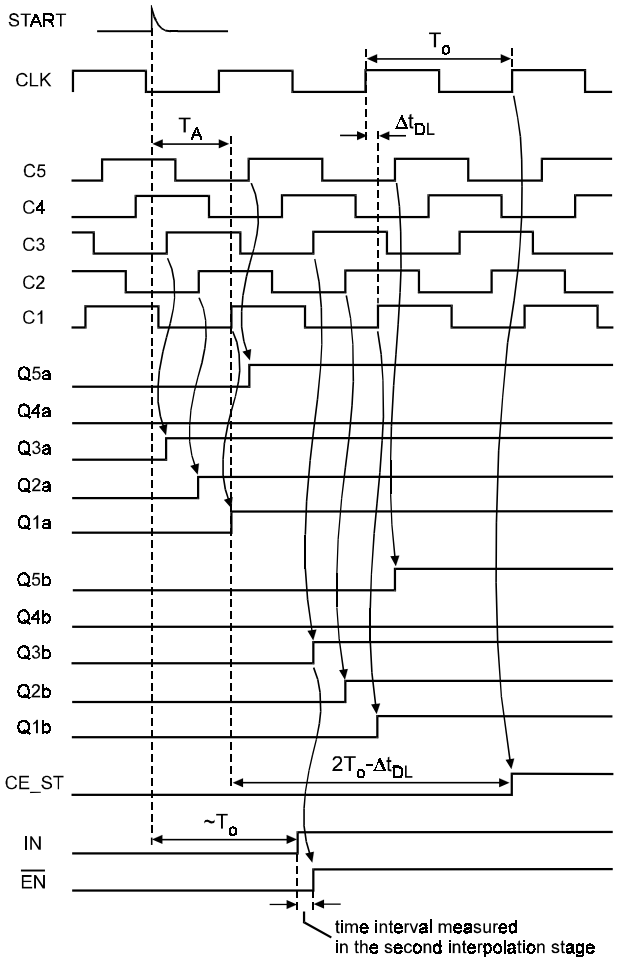

Fig. 2 Example of waveforms in the START interpolator

3. Test results

Tests of the programmed FPGA were performed under computer control, using custom designed user interface and a statistical software written in *Borland Delphi*. To determine the resolution and the non-linearity of interpolators, we used the well known statistical method involving a large number of measurements of random time intervals having uniform distribution within the period T_0 [7]. Since each cell in the first interpolation stage determines a number of active delay cells in the second stage (differential delay line), the full differential non-linearity characteristic of the time-to-digital converter can be obtained by concatenation of five conversion characteristics of the second interpolation stage.

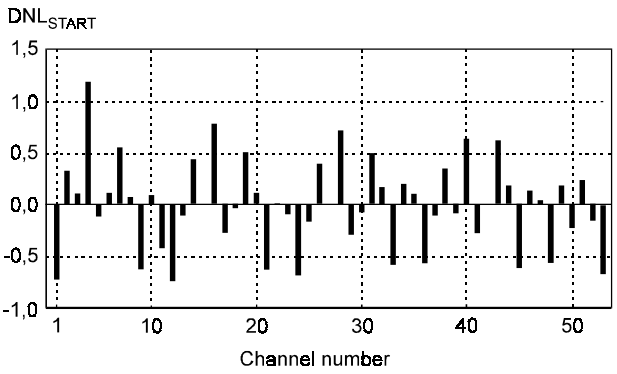

Fig. 3 Differential non-linearity of START interpolator

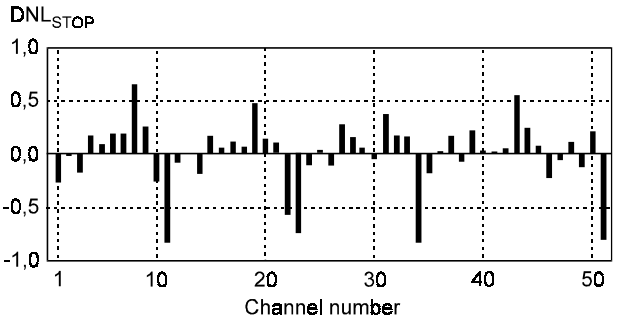

Fig. 4 Differential non-linearity of STOP interpolator

In the START interpolator 53 quantization steps were obtained (Fig. 3), resulting in the average resolution $LSB_{START} = T_0/53 = 189$ ps. In the STOP interpolator $LSB_{STOP} = 196$ ps at 51 quantization steps was obtained (Fig. 4). Maximum integral non-linearity (INL) equal to 1.65 $LSB_{START} = 312$ ps and 1.1 $LSB_{STOP} = 216$ ps was calculated for respective interpolators. These values are about three times lower than those obtained in the time counter with single interpolation, using the same FPGA device [1]. To lower the linearity errors, we used for each interpolator the values of the respective INL function as a correction vector [1, 2, 7, 12]. In this way the integral non-linearity has been limited to ± 0.1 LSB in both interpolators.

Because in the time counters based on the Nutt method the behavior of the "random error" or the standard measurement uncertainty is periodical (modulo clock period) [7], we measured ten constant time intervals generated asynchronously with regard to the reference clock and incremented by 1 ns. We used ten coaxial cables of suitable lengths to set the measured time intervals. Fig. 5 shows the standard deviation (or standard uncertainty) calculated for each sample at a given delay with the enabled and disabled non-linearity correction of both interpolators. It should be noted that even without correction the standard measurement uncertainty is not greater than the resolution of interpolators.

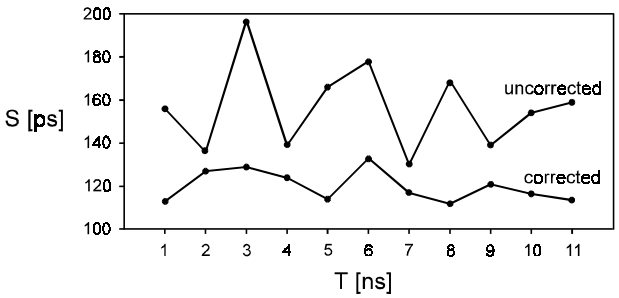

Fig. 5 Standard deviation *S* of time intervals within the clock reference period (10 ns)

The standard uncertainty calculated within the full measurement range of the designed time counter is shown in Fig. 6. A Stanford Research DG535 delay generator was used as a time interval source. The increasing of the standard uncertainty at long time intervals is caused by the cumulative short-term error of the clock generators used in the DG535 and the tested counter.

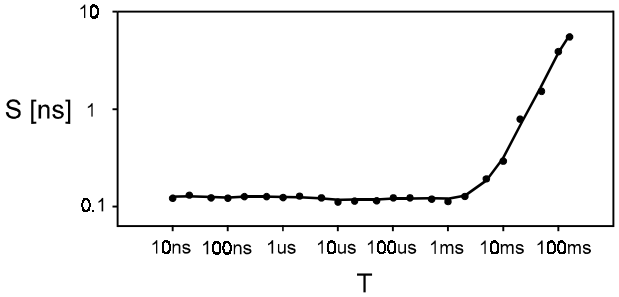

Fig. 6 Standard deviation *S* of time intervals within the full measurement range of the counter (167 ms)

References

[1] J. Kalisz, R. Szplet, R. Pełka, A. Poniecki, "Single-chip interpolating time counter with 200-ps resolution and 43-s range", IEEE Trans. Instrum. Meas., Vol. 46, No. 4, August 1997, pp. 851-856

[2] R. Szplet, J. Kalisz, R. Szymanowski, "Interpolating time counter with 100 ps resolution on a single FPGA device", IEEE Trans. Instrum. Meas., Vol. 49, No. 4, August 2000, pp. 879-882

[3] M. S. Andaloussi, M. Boukadoum, E. Aboulhamid "A novel time-to-digital converter with 150 ps time resolution and 2.5 ns pulse-pair resolution", Proc. 14th Int. Conf. Microelectronics ICM2002, pp. 123-126

[4] M. Zieliński, D. Chaberski, M. Kowalski, R. Frankowski, S. Grzelak, "High-resolution time-interval measuring system implemented in single FPGA device", Measurement, Vol. 35, Issue 3, April 2004, pp. 311-317

[5] J. Wu, Z. Shi, Y. Wang, "Firmware-only implementation of Time-to-Digital Converter (TDC) in Field-Programmable Gate Array (FPGA)", Nucl. Sci. Symp., Portland, 2003

[6] A. Mäntyniemi, T. Rahkonen, J. Kostamovaara, "A high resolution digital CMOS time-to-digital converter based on nested delay locked loops", Proc. IEEE Int. Symp. Circuits and Systems ISCAS'99, July 1999, Vol. II, pp. 537-540

[7] J. Kalisz, "Review of methods for time interval measurements with picosecond resolution", Metrologia (41), 2004, pp. 17-32

[8] R. Szymanowski, "Metastability effects in a two-stage time interpolator", Metrology and Measurement Systems, Vol. X, No. 3, 2003, pp. 319-329

[9] C. Ljuslin, J. Christiansen, A. Marchioro, O. Klingsheim, "An integrated 16-channel CMOS time to digital converter", IEEE Trans. Nuclear Sci., Vol. 41, No. 4, August 1994, pp. 1104-1108

[10] A. Mäntyniemi, T. Rahkonen, J. Kostamovaara, "A 9-channel integrated time-to-digital converter with sub-nanosecond resolution", Proc. Midwest Symp. of Circuits and Systems, August 1997, pp. 189-192

[11] J. Kalisz, T. Orżanowski, R. Szplet, "Delay-locked loop technique for stabilization of internal delays of CMOS FPGA devices", Electronics Letters, Vol. 36, No. 14, 6th July 2000, pp. 1184-1185

[12] R. Pełka, J. Kalisz, R. Szplet, "Nonlinearity correction of the integrated time-to-digital converter with direct coding", IEEE Trans. Instrum. Meas., Vol. 46, No. 2, April 1997, pp. 449-452