J. Opt. **29** (1998) 199–205. Printed in the UK PII: S0150-536X(98)91711-7

Single-chip low-cost time counter for distance measurements with 3 cm resolution

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Received 1 October 1997

Abstract. A new design of fully integrated time counter is presented for application in laser ranging systems with 3 cm resolution. The counter is implemented on a single FPGA chip with amorphous antifuse structures. The counter contains two time-to-digital converters, each having 200 ps resolution least-significant bit (LSB) within a 10 ns range and a 32-bit, 100 MHz real-time counter. The control software and a versatile user interface, developed with the aid of the Delphi tools, are also described. At an ambient temperature of +20 °C we achieved a random error of 129 ps or 0.65 LSB. This is equivalent to a random error in the distance measurement equal to about 2.1 cm. The power consumption of the integrated counter is 5.2 mW when the clock is disconnected, which rises to about 390 mW in the active mode.

Keywords: Time counters, time-to-digital converters, delay verniers, digital delay lines

Un compteur de temps intégré économique pour les mesures de distance avec une résolution de 3 cm

Résumé. Un nouveau design d'un compteur d'intervalles de temps entièrement intégré est présenté pour des applications dans les systèmes laser de mesure de distance avec une résolution de 3 cm. Le compteur est implanté dans un circuit FPGA à structures amorphes 'antifuse'. Le compteur contient deux convertisseurs temps–chiffre possédant chacun la résolution de 100 ps du bit le moins significatif (LSB) dans l'intervalle de 10 ns et un compteur temps-réel de 32 bits, 100 MHz. Sont également décrits: le logiciel de contrôle et l'interface flexible utilisateur développés avec DELPHI. A température ambiante de 20 °C nous avons obtenu l'erreur aléatoire de 129 ps soit 0,65 LSB, ce qui correspond à une erreur de distance d'environ 21 mm. La consommation d'énergie du circuit intégré est de 5,2 mW avec l'horloge 100 MHz déconnectée augmentant jusqu'à 390 mW en mode actif.

Mots clés: Convertisseurs temps–chiffre, compteurs d'intervalles de temps, lignes à retard numériques

1. Introduction

Distance measurement in laser ranging systems is accomplished by measurement of the time of flight of the laser pulse travelling to the target and back. To obtain high measurement accuracy the time counter used should feature small quantization steps (incremental resolution or least-significant bit (LSB)), low random and systematic errors and a short dead time.

To reduce dimensions, power consumption and cost, modern time counters utilize the *direct time-to-digital conversion* principle involving the use of integrated, tapped delay lines, as opposed to classic designs based on *indirect* time-to-amplitude/amplitude-to-digit conversion,

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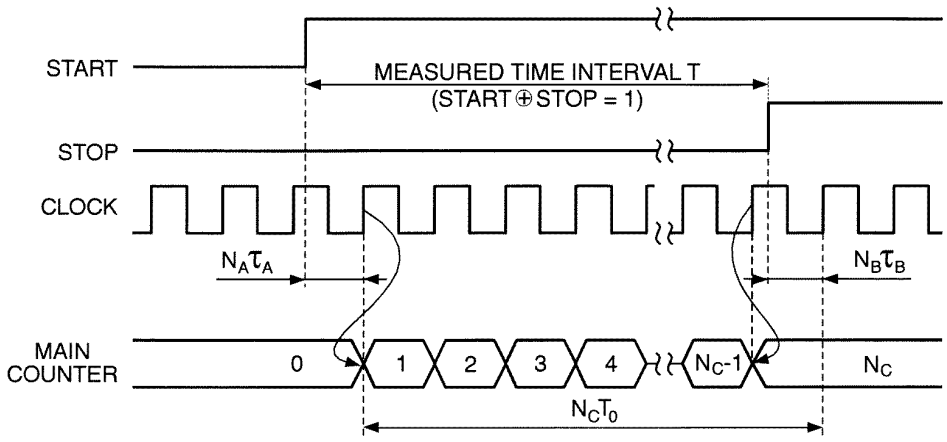

Figure 1. Interpolation method for precise measurement of time intervals.

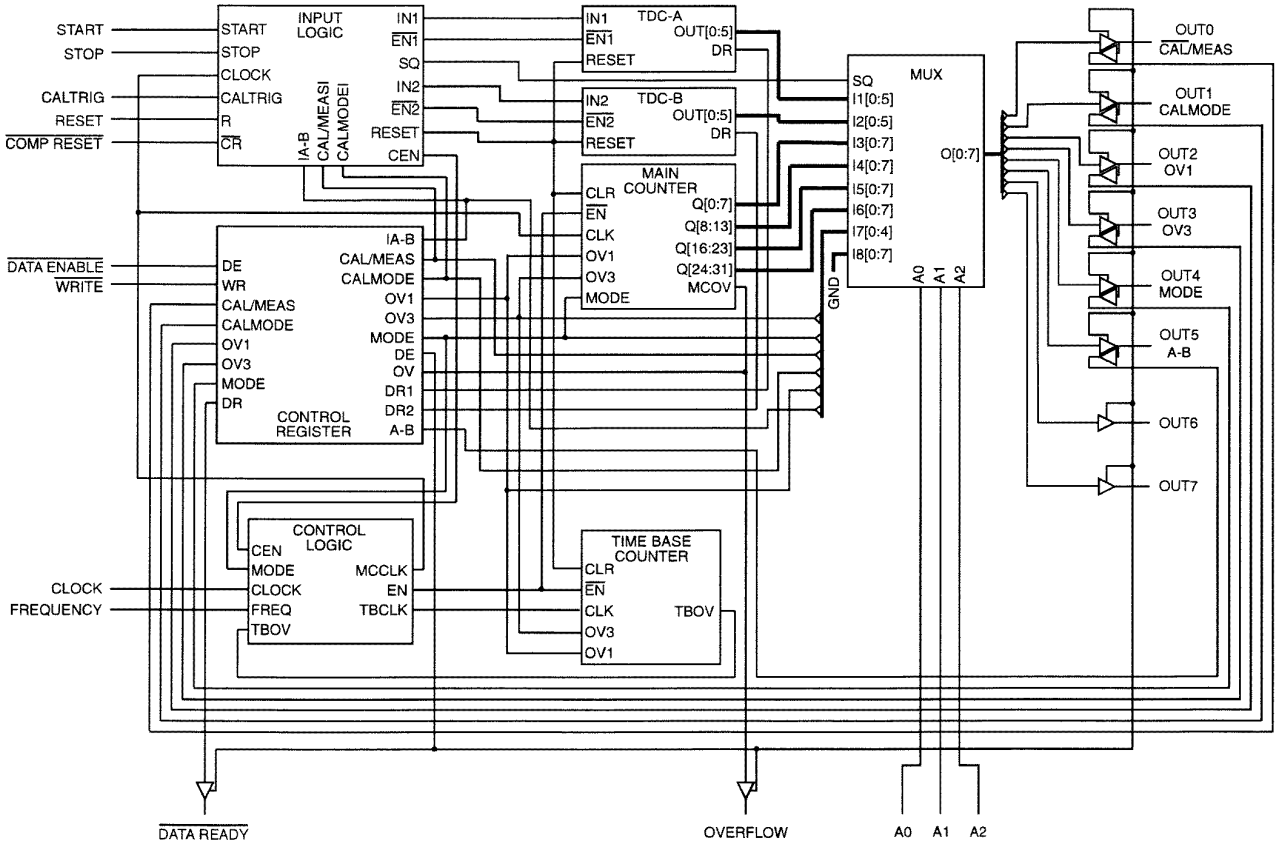

Figure 2. Simplified logic diagram of the time counter.

or the time-expansion/time-counting principle. The lowest resolution may be obtained using two delay lines working in *differential* mode, with the logic schemes proposed in [1, 2]. The other similar approach is based on the *pulse shrinking* principle [2, 3]. For this purpose, however, using the technology of custom or semi-custom integrated circuits would mean high cost and only a limited possibility of design refinement.

In this application, the use of the field-programmable gate array (FPGA) technology ushers in new possibilities for the development of fast and cost-effective time counters. We have shown [4] that using the 0.65 μm CMOS FPGA technology with amorphous antifuse structures [5] one can create an interpolating time counter with 200 ps resolution and 43 s range. Since the high-resolution time coding is realized directly by the integrated delay lines, the counter features very short conversion time.

In this paper we describe the design of this time counter and its control software for distance measurement. The counter is implemented on the FPGA chip with

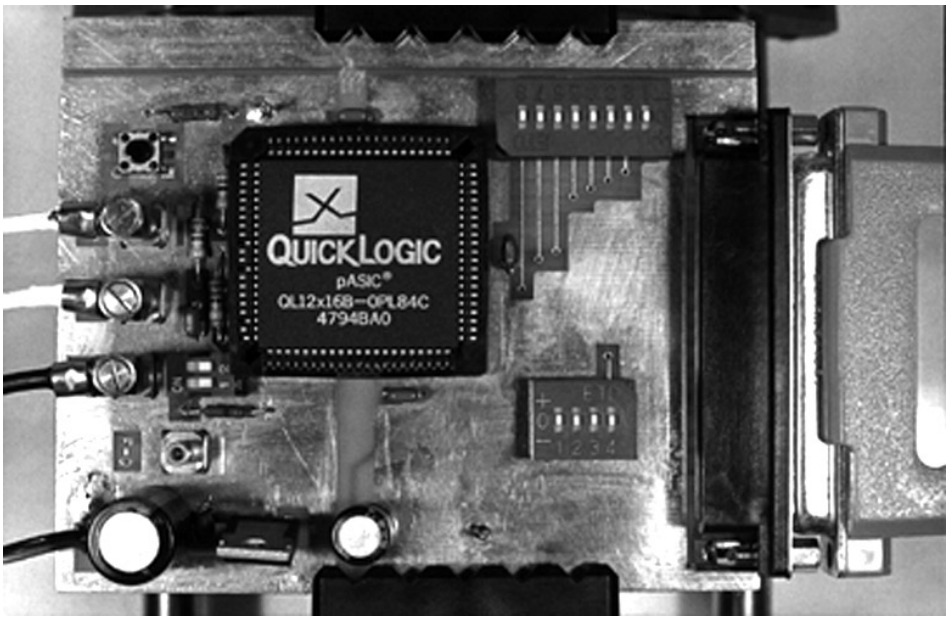

Figure 3. Dedicated board for testing the time counter.

pASIC architecture [5] and contains two 6-bit time-to-digital converters (TDC) of design similar to that described in [6], two multibit synchronous counters operating at 100 MHz, a control register and input/output circuits. The counter is complemented with control software based on Borland's Delphi tools and a dedicated interface for the IBM compatible computer. The counter may also be controlled by a typical single-chip microcontroller driving the display and/or an external interface.

2. Design of the time counter

The design of the counter is based on the classic interpolation method described by Nutt [7, 8]. It involves splitting the measured time interval T into three parts, the first being the integer number N_C of reference clock periods T_0, and two short intervals (at the initial and final part of the measured interval), each having a duration of less than one clock period (figure 1). The first part ($N_C T_0$) is measured by the synchronous, 32-bit binary counter to 10 ns accuracy (at 100 MHz), while the remaining two parts ($N_A \tau_A$ and $N_B \tau_B$) are measured with the aid of two TDCs with quantization steps τ_A and τ_B, respectively. Neglecting the conversion error of the TDCs

$$T = N_B \tau_B - N_A \tau_A + N_C T_0 \qquad (1)$$

and the maximum measured time interval is $T_0\left(2^{32}-1\right) \approx$ 43 s. The time-to-digital conversion in each TDC is realized directly by the time-coding line consisting of two tapped delay lines working in differential mode [4]. The complete time-coding line contains 63 delay cells divided into three segments. The useful segment contains about 50 cells of total time span equal to the single period of the reference clock (10 ns at 100 MHz) and is located approximately in the middle of the coding line to account for the time and temperature drift of the TDC. The initial offset segment contains typically eight cells and the final segment contains the remaining cells. The converters also contain the calibration circuits and the phase detectors needed in the interpolation process.

The counter has been designed to achieve $\tau_A \approx \tau_B \approx$ 200 ps. This corresponds to a quantization step in the distance measurement of about 3 cm. Figure 2 shows the simplified block diagram of the integrated time counter. The time interval T is measured between the rising edges of the input pulses START and STOP. To select the working mode of the TDC, the MODE word is loaded into the internal, 6-bit control register. The 6-byte output data (four bytes from the main counter and two from the TDCs) can be read consecutively by changing the 3-bit address of the 7-to-1 byte multiplexer array. In addition, the content of the control register can be read for test purposes. The three-state bidirectional I/O buffers allow reading the output data and loading the input MODE data into the control register using the same pins. The design and programming of the FPGA devices were accomplished with the aid of the firmware SpDE version 4.23 [5]. We achieved a chip utilization ratio of 93.2%.

3. Experimental set-up

We accomplished the tests of the designed time counter with the use of a dedicated board (figure 3). The board is connected to the PC controller by the multiwire flat cable and another dedicated interface card plugged into the ISA bus slot of the computer. The interface contains two bidirectional bus buffers and additional logic (address decoders) implemented in a single PLD chip (GAL 20V8).

We also designed a second version of the interface for the Intel 80C51 single-chip microcontroller which may be used in mobile applications of the distance meter. Both

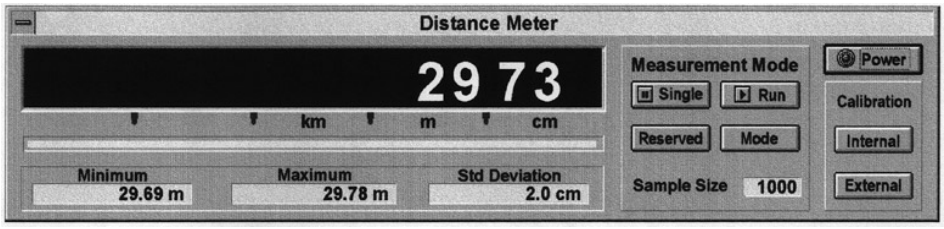

Figure 4. Screen snapshot of the user interface.

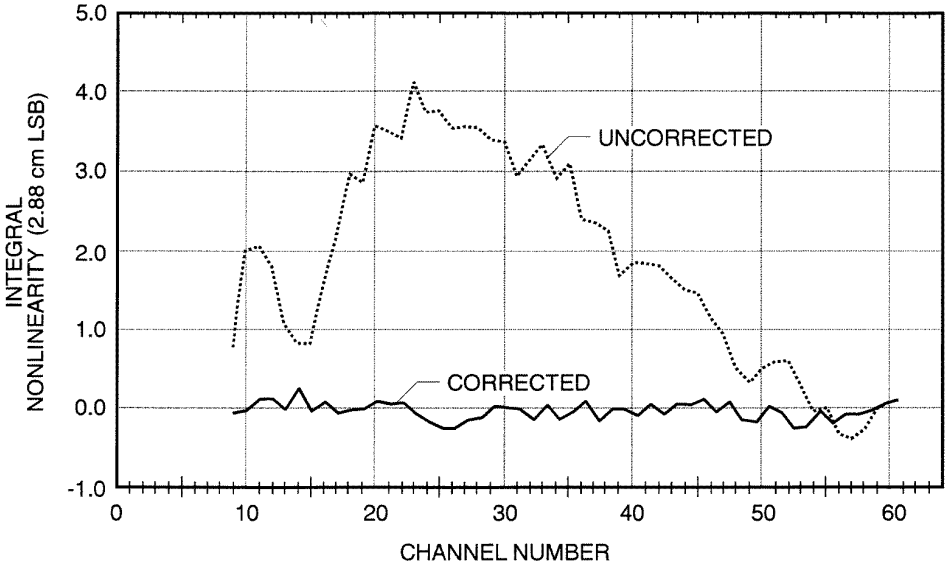

Figure 5. Plots of the corrected and uncorrected integral nonlinearity of TDC A.

versions of the control system feature all the functions necessary for setting the working mode of the time counter, diagnostics, data processing and display of the measurement results.

The software for the IBM PC platform may run on any computer supporting the Windows 3.1 or Windows 95 operating system. It has been developed using Borland's C++ 5.0 compiler and the Delphi rapid application development tools. The software consists of five parts compiled as DLL units:

(i) hardware control for writing to and reading from the internal registers of the time counter;
(ii) test tools, consisting of a set of procedures for calibration purposes, for calculating the nonlinearity errors of the two TDCs, and for processing the measurement results;
(iii) graphics tools, for visualization of the data in the form of plots and histograms;
(iv) data management, in the form of an optional DLL for saving and loading data to/from disk files, for exchanging graphics with Windows applications like Corel Draw and for exporting the data files into the Paradox 7.0 format for further processing;
(v) a graphical user interface, for interactive communication based on the windows dialog system.

A full version of the software supporting all diagnostics and data postprocessing functions requires 3.5 MB of disk space and consists of the executable file and three DLLs. In the simplified version featuring only the basic functions of the virtual instrument, without the detailed analysis of the nonlinearity errors, just one DLL is needed. Figure 4 shows a snapshot of the screen interface in the distance measurement mode. Other measurement modes include: time interval measurement, cable length measurement and frequency measurement. User procedures for calculation of measurement results using specific constants and corrections may be easily linked as separate DLLs.

4. Experimental results

We first tested the nonlinearity error of both TDCs contained in the counter using the samples of 500 000 measurements of time intervals of random duration. For TDC A we obtained a maximum differential nonlinearity error of 1.115 LSB or 214 ps and for TDC B similar values of 0.975 LSB or 187 ps. The maximum integral nonlinearity error of TDC A was 4.2 LSB or 806 ps and for TDC B we obtained 4.0 LSB or 768 ps. Although the integral nonlinearity errors of TDC A and TDC B may cancel each other to a certain extent during the interpolation process, their values are significant and should be reduced by an appropriate self-correction procedure. The random

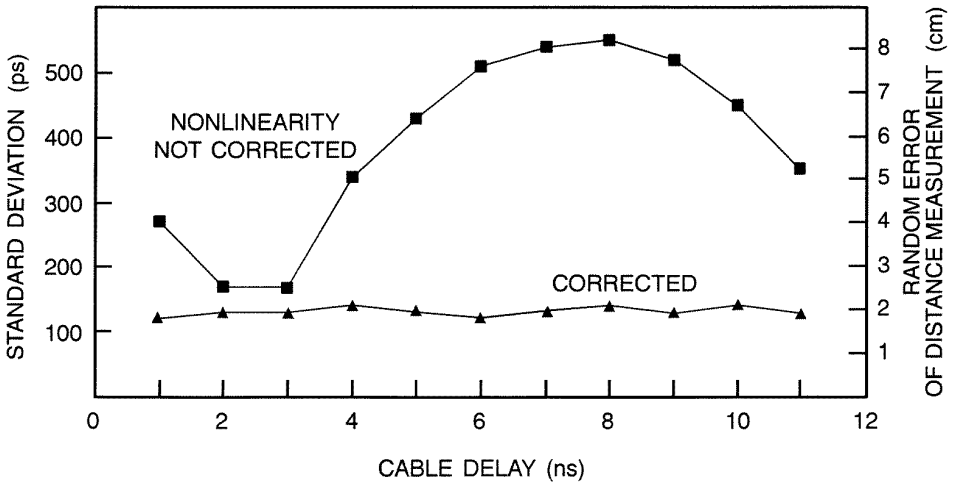

Figure 6. Random error obtained with and without correction of the TDC's nonlinearity.

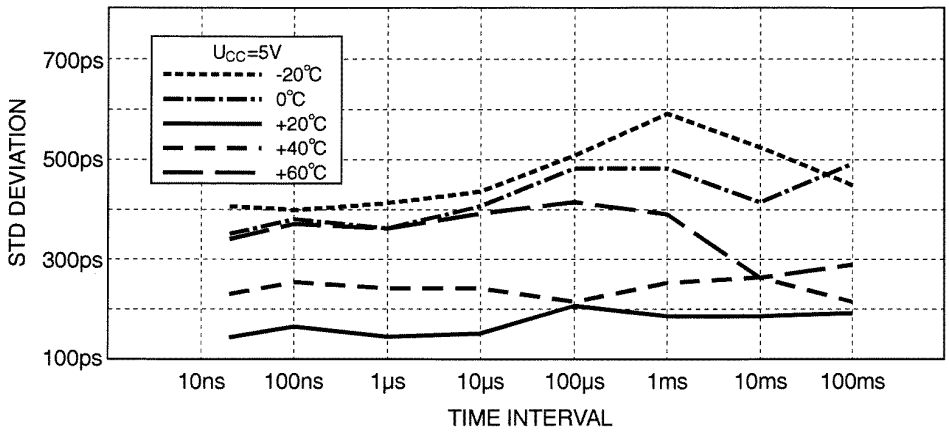

Figure 7. Random error of the counter as a function of the measured time interval and the ambient temperature.

error caused by the quantization may be estimated as $200\ \text{ps}/\sqrt{12} \approx 58$ ps.

In order to diminish the nonlinearity error we tested a number of procedures for self-correction of that error. The simplest method uses a constant correction term which is subtracted from the TDC output data. If the correction term is assumed as one half the sum of the maximum and minimum values of the integral nonlinearity, the maximum integral nonlinearity error of each TDC may be reduced twice. Much more accurate correction is possible when the values of the integral nonlinearity function at each output channel of the TDC are used as correction vectors [8, 9]. Figure 5 shows the effectiveness of this method applied to the TDC A. As may be seen, the nonlinearity error has been lowered dramatically to 0.24 LSB or 46 ps, which is equivalent to an uncertainty of about 0.7 cm for distance measurements.

We also tested the correction procedure by collection and evaluation of a sample of measurements of a constant time interval (the fixed delay of the coaxial cable), generated asynchronously with respect to the reference clock. For the sample of 5000 measurements we obtained a standard deviation equal to 351 ps and after correction it was reduced to 129 ps or 0.65 LSB, assuming 1 LSB = 200 ps. Again relating this error to the distance measurement we get an equivalent random error of about 2.1 cm.

To verify the accuracy of the counter over the full dynamic range of the TDCs (a single clock period or 10 ns) we used the set of 11 precisely cut coaxial cables, with delays differing by 1.0 ns. For each cable we measured the mean value of its delay by our counter and by the commercial time counter SR620 (Stanford Research Systems) featuring 4 ps resolution and 25 ps random error (RMS). We obtained a maximum difference of 72 ps. The plots shown in figure 6 illustrate the standard deviation of the measurement data of our counter within the same measurement range obtained with correction of the TDC's nonlinearities, and without the correction.

We also examined the temperature stability of the time counter over the ambient temperature range from $-20\,^{\circ}$C to $+60\,^{\circ}$C. We calculated the standard deviation of measured delays varying from 20 ns to 100 ms using the sample size of 5000 measurements for each delay. The correction vector for nonlinearity error compensation was calculated only once at the temperature $t_{\text{amb}} = +20\,^{\circ}$C. Plots of the

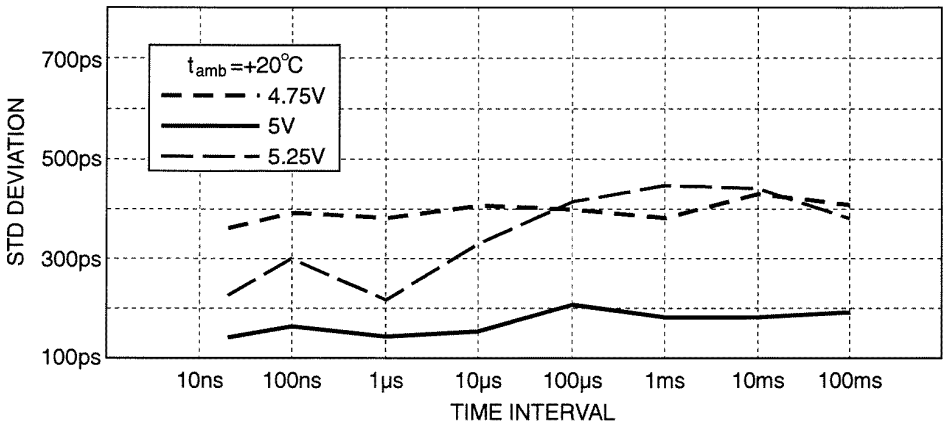

Figure 8. Random error of the counter as a function of the measured time interval and the power supply voltage.

Table 1. The main features of the FPGA time counter.

Time range	0–43 s
Time resolution (LSB)	$\sim$ 200 ps
Random error (RMS) at (0–100 ms) range	$<$200 ps at t_{amb} = +20 °C $<$600 ps at t_{amb} = −20 to +60 °C $<$450 ps at U_{CC} = 4.75–5.25 V
Integral nonlinearity of a single TDC	$<$4 LSB or 800 ps (without correction) $<$0.25 LSB or 50 ps (with correction)
Modes of operation	A $\rightarrow$ B with Start channel distinction A $\leftrightarrow$ B without Start channel distinction
Frequency measurement	up to 105 MHz
Time base clock	100 MHz (10 ns clock period)
Power supply	+5 V
Power consumption	390 mW in operating mode 5.2 mW in standby mode
Technology	0.65 μm CMOS FPGA (QuickLogic)
Package	PLCC, 84-pin

calculated random error are shown in figure 7.

As expected, we obtained the smallest standard deviation at the temperature $t_{amb} = +20\,^{\circ}C$, when the nonlinearity correction is most effective. In this case the maximum standard deviation equals 210 ps at the time interval $T = 100\ \mu s$. The worst value of standard deviation equal to 590 ps was obtained at the time interval $T = 1$ ms and the temperature $t_{amb} = -20\,^{\circ}C$. In a similar way we tested the influence of the power supply voltage on the random error of the time counter by changing that voltage by ± 0.25 V around the nominal value of $+5$ V (figure 8). Obviously, the bottom plot in figure 8 obtained at $U_{CC} = +5$ V is the same as the bottom plot in figure 7. The worst-case error appears at $U_{CC} = +5.25$ V and $T = 1$ ms. The main features of the FPGA time counter are summarized in table 1.

5. Conclusions

The integrated time counter may be used for developing high-precision, small-size and cost-effective laser ranging systems even in small quantities. The resolution is 3 cm at any measuring range in terrestrial or spaceborne applications. The user-friendly control software developed for the Windows/PC platform includes a graphical interface and procedures for calibration, diagnostics and data processing. A single-chip microcomputer control may be used for applications in mobile or portable distance meters.

Acknowledgment

This work was supported by the Polish Science Council (KBN) under contract no 120/E-410/F/97.

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